WLAN - 802.11 Chipset Power Supply Implementation Using the ISL6413

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ISL6413 Triple Output Regulator with Single Synchronous Buck and Dual LDO

The ISL6413 is a highly integrated triple output regulator which provides a single chip solution for wireless chipset power management. The device integrates a high efficiency synchronous buck regulator with two ultra low noise LDO regulators and a RESET. It accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (PWM), 2.84V (LDO1), and another ultra low noise 2.84V (LDO2). The PWM output maintains regulator down to 2.7V input voltage.

The PWM regulator is a current mode control synchronous buck regulator with integrated N- and P- channel power MOSFETs. It's output is pre-set to 1.8V for the BBP/MAC core supply. Synchronous rectification with internal MOSFETs achieves >92% efficiency. The operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates any loss of regulation on the PWM output.

The ISL6413 also has two LDO regulators which use internal PMOS transistors as the pass devices. LDO2 features ultra low noise that typically does not exceed $30\mu V_{RMS}$ to aid VCO stability. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6413 also integrates a RESET function, eliminating the need for an additional RESET IC usually required in WLAN applications. This function asserts a RESET signal whenever the VIN supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after VIN has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Additional features include over current protection for all three outputs and thermal shutdown.

High integration , excellent efficiency and the thin, Quad Flat No-lead (QFN) package makes the ISL6413 an ideal choice to power many of today's small form factor industry standard wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

ISL6413 Reference Design

The ISL6413 evaluation board highlights the operation of the IC in an embedded application.

TABLE 1. EVALUATION BOARDS

BOARD NAME	IC	PACKAGE
ISL6413EVAL1	ISL6413IR	24 Ld QFN

Quick Start Evaluation

The evaluation board is shipped "ready to use" right from the box. The board accepts a 3.3V input from a standard power supply. The output can be exercised through the use of an external load.

There are posts available on the board for introducing power, for drawing current from the regulated output, and also for testing other functions like RESET, SYNC, Power Good and Shutdown.

Recommended Test Equipment

- A 3.3V, 2A capable power supply
- An electronic load 3 channels
- A four-channel oscilloscope
- Precision digital multimeters

Power and Load Connections

There are 2 sets of terminals that are used for supplying the input power and 3 sets of terminals used for loading the 3 outputs (1 PWM and 2 Linear regulators).

Input Voltage - Connect the positive lead of the power supply to V_{IN} (P1) post and V_{IN}_LDO (P11) post and the ground lead of the supply to the PGND (P2) post and the GND_LDO (P10) post.

Output Loading, Sourcing Current - To load the PWM output, connect the positive lead of the electronic load to the V_{OUT} (P6) post and the return terminal of the same load channel to the PGND (P7) post. Similarly, connect the positive terminal of the second load channel to the V_{OUT1}(P9) post and the return terminal to the GND_LDO (P12) post to load the output of LDO1. The ultra low noise LDO2 output can be loaded by connecting the positive terminal of a third channel of the electronic load to the V_{OUT2} (P8) post and the return terminal to the GND_LDO (P12) post.

Startup

There are two distinct start up methods for the ISL6413. The first method is by the application of power to the inputs of the IC. A controlled turn on of the outputs is allowed by the soft-start feature of the IC. The soft start duration for the PWM is typically 5.5ms with 750kHz switching frequency. The soft-start duration for LDOs is 120µs.

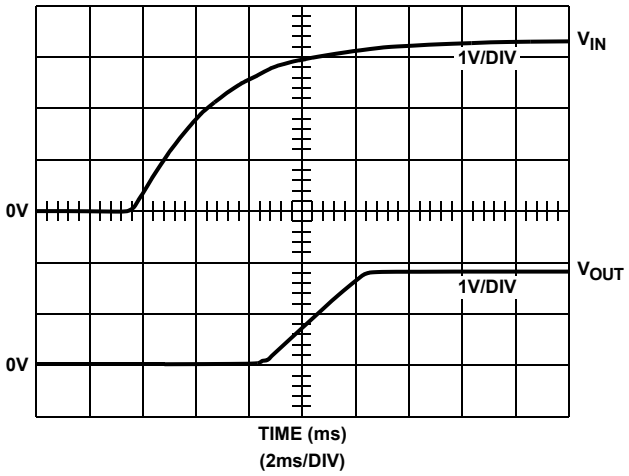


FIGURE 1. PWM SOFT-START WAVEFORM

The second method of startup is by using the Enable feature on the PWM and LDO outputs. The output of the PWM is enabled when the EN_PWM pin is floating or pulled HIGH and disabled when the pin is pulled to ground. Similarly, holding the EN_LDO pin on the ISL6413 LOW or pulled to ground will disable both LDO outputs. Releasing the pin allows the LDOs to start up.

Shutdown

As discussed in the previous section, the PWM regulator can be shutdown by pulling the EN_PWM pin to ground; the LDO regulators can be shutdown by pulling the EN_LDO pin to ground.

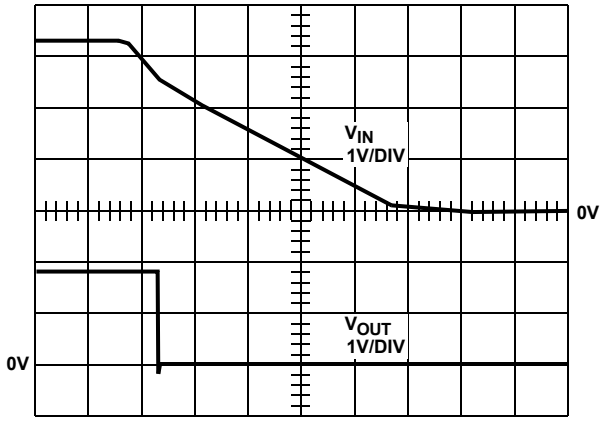


FIGURE 2. PWM SHUTDOWN WITH V_{IN}

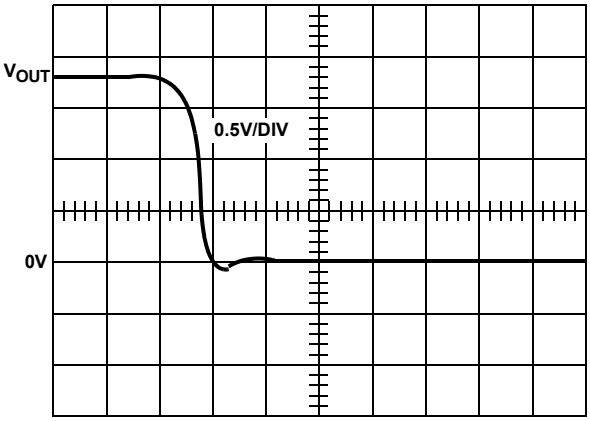


FIGURE 3. PWM SHUTDOWN WITH EN_PWM

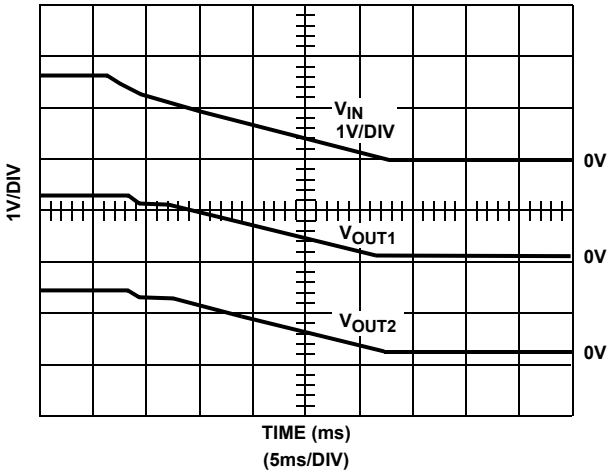


FIGURE 4. LDO SHUTDOWN WITH V_{IN}

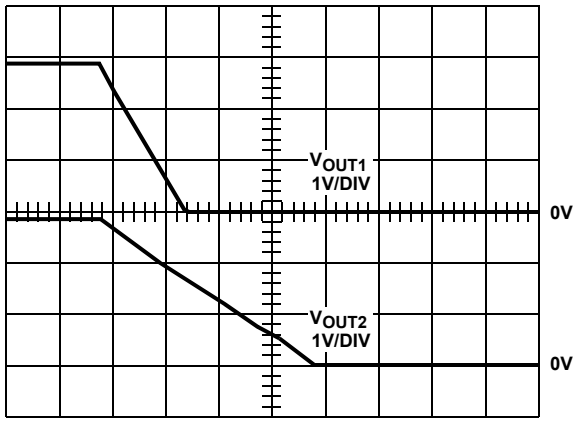


FIGURE 5. LDO SHUTDOWN WITH EN_LDO

Output Performance

The ISL6413 provides fixed output voltages for use in Wireless Chipset applications. Internal trimmed resistor networks set the typical output voltages as V_{OUT_PWM} = 1.8V; V_{OUT1} = 2.84V and V_{OUT2} = 2.84V. All three outputs have excellent line/load regulation and transient response as shown in figure 7 to 12.

The PWM switching frequency is typically 750kHz and the device can be synchronized to an external frequency in the range of 500kHz to 1MHz by connecting an external clock source to the SYNC pin. The PWM output ripple is as shown in figure 6. The LDO2 output features ultra low noise, typically <30µV RMS, to facilitate VCO stability.

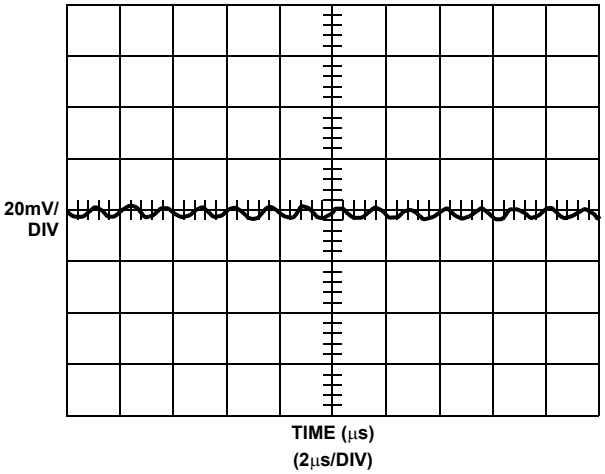


FIGURE 6. PWM OUTPUT RIPPLE WAVEFORMS

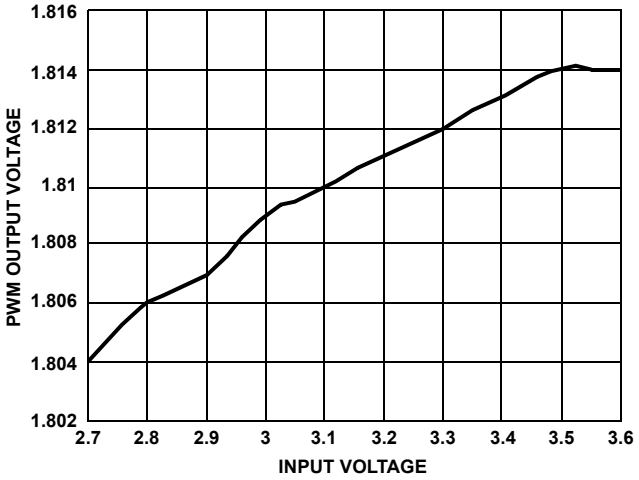


FIGURE 7. PWM LINE REGULATION

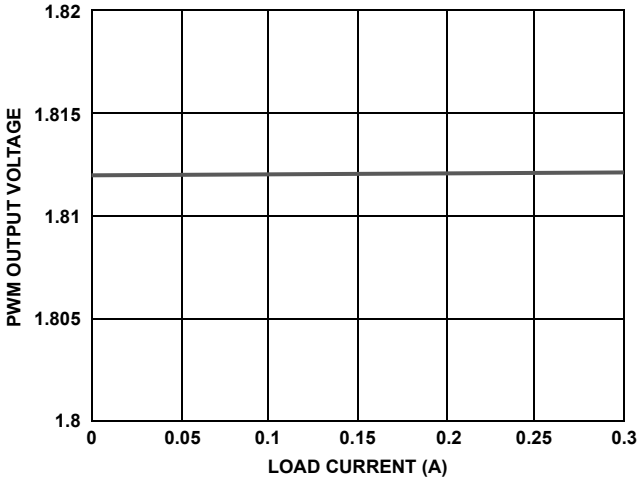


FIGURE 8. PWM LOAD REGULATION

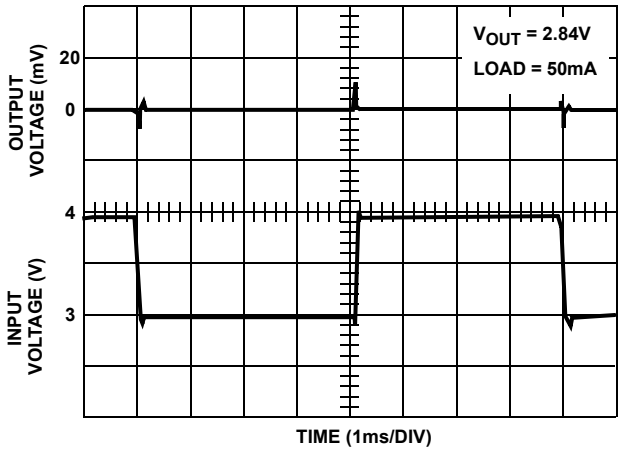


FIGURE 9. LINE REGULATION RESPONSE ($V_{OUT}1$)

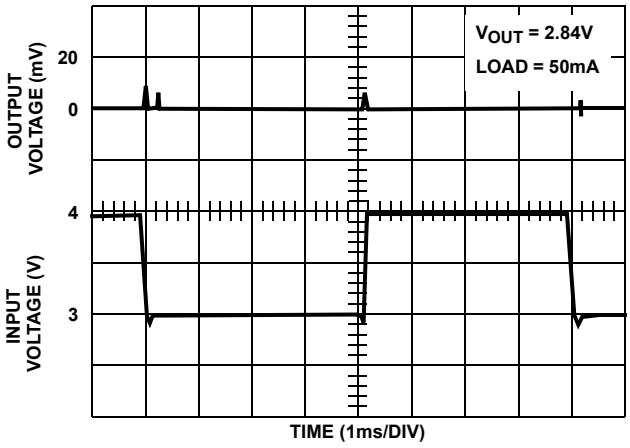


FIGURE 10. LINE REGULATION RESPONSE ($V_{OUT}2$)

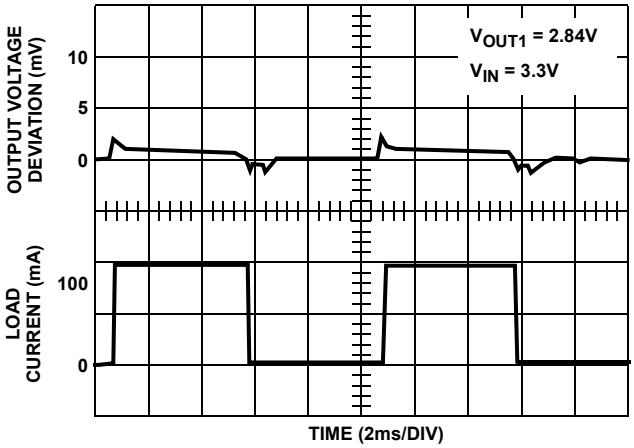


FIGURE 11. LOAD REGULATION RESPONSE ($V_{OUT}1$)

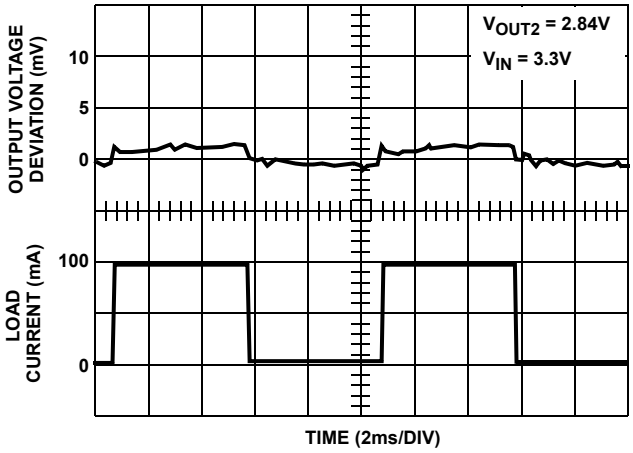


FIGURE 12. LOAD REGULATION RESPONSE ($V_{OUT}2$)

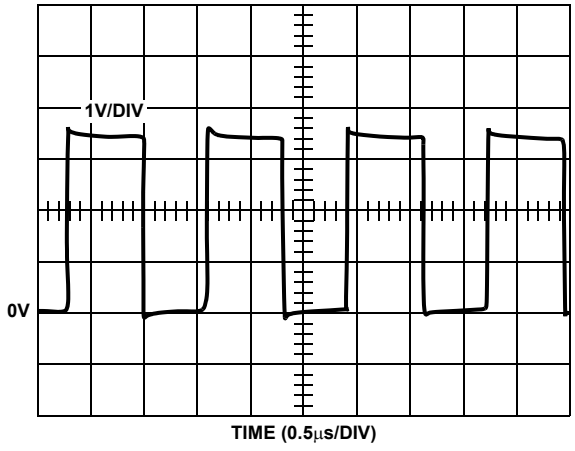


FIGURE 13. PWM PHASE NODE SWITCHING

Power Saving with PWM Supply for BBP/MAC

The ISL6413 offers significant power savings compared to a LDO based 1.8V BBP/MAC power supply. Figure 14 shows the efficiency comparison between PWM and LDO outputs for 1.8V supply.

For a typical 300mA current drawn from the 1.8V output by the BBP/MAC on the 1.8V output, the PWM efficiency will be close to 92% and the Input current drawn from the 3.3V supply will be:

$I_{IN(PWM)}$ = (1.8V x 300mA) / (3.3V x 0.92) = 178mA

For the same 300mA output current drawn by BBP/MAC on LDO based 1.8V output supply, the LDO efficiency will be 54% and the Input current drawn from the 3.3V supply will be 300mA.

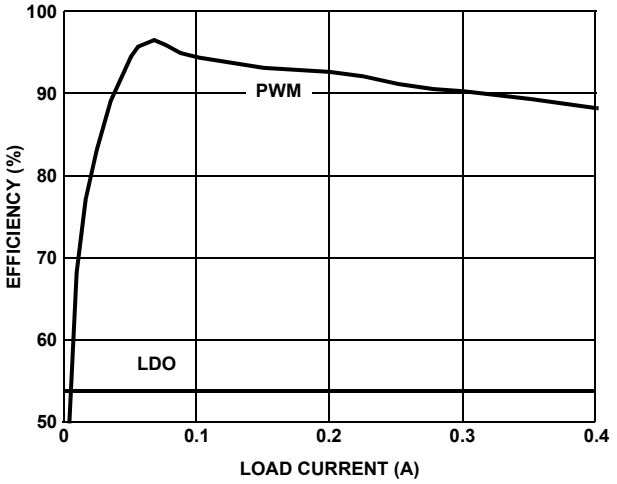


FIGURE 14. PWM AND LDO EFFICIENCY vs LOAD CURRENT

Hence, the ISL6413 reduces the supply current by about 120mA, saving 400mW of power compared to the LDO option for the 1.8V BBP/MAC power supply at a typical 300mA load. This power saving and efficiency improvement not only improves system battery life but offers better thermal performance due to reduced on-chip power dissipation.

For high efficiency applications where battery life is critical, the ISL6413 is recommended, whereas the ISL6411 is recommended for low cost applications.

Functional Description

Synchronous Buck Regulator

The synchronous buck regulator with integrated N- and P-channel power MOSFETs provides pre-set 1.8V for BBP/MAC core supply. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz, allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of

500kHz to 1MHz. The PG_PWM output indicates loss of regulation on the PWM output.

The PWM architecture uses a peak current mode control scheme with internal slope compensation. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The error amplifier sets the threshold for the PWM comparator. The high side switch is turned off when the sensed inductor current reaches this threshold. After a minimum dead time, preventing shoot through current, the low side N-channel MOSFET will be turned on and the current ramps down again. As the clock cycle is completed, the low side switch will be turned off and the next clock cycle starts.

The control loop is internally compensated, reducing the amount of external components. The PWM section includes an anti-ringing switch to reduce noise at light loads.

The switch current is internally sensed and the minimum current limit is 550mA.

Frequency Synchronization

The typical operating frequency for the converter is 750kHz if no clock signal is applied to the SYNC pin. It is possible to synchronize the converter to an external clock within a frequency range from 500kHz to 1MHz. The device automatically detects the rising edge of the first clock and will synchronize immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation without interruption. The switch over will be initiated if no rising edge on the SYNC pin is detected for a duration of two internal 1.3µs clock cycles.

PWM Soft Start

As the EN_PWM (Enable) pin goes high, the soft-start function will generate an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typically 5.5ms with 750kHz switching frequency. When the soft-start is completed, the error amplifier will be connected directly to the internal voltage reference. The SYNC input is ignored during soft start.

Power Good (PG_PWM)

When the chip is enabled, this output is HIGH when V_{OUT} is within 8% of 1.8V and active low outside this range. When the PWM is disabled, the output is active low. $\overline{PG\_PWM}$ is the complement of PG_PWM.

Leave the PG_PWM pin unconnected when not used.

PWM Overvoltage and Overcurrent Protection

The PWM output current is sampled at the end of each PWM cycle. Should it exceed the overcurrent limit, a 4 bit up/down counter counts up two LSB. Should it not be in overcurrent the counter counts down one LSB (but the counter will not "rollover" or count below 0000). If >33% of the PWM cycles go into overcurrent, the counter rapidly reaches count 1111 and the PWM output is shut down and the softstart counter is reset. After 16 clocks the PWM output is enabled and the SS cycle is started.

If V_{OUT} exceeds the overvoltage limit for 32 consecutive clock cycles, the PWM output is shut off and the SS counters reset. The softstart cycle will not be started until EN or V_{IN} are toggled.

LDO Regulators

Each LDO consists of a 1.184V reference, error amplifier, MOSFET driver, P-Channel pass transistor, dual-mode comparator and internal feedback voltage divider.

The band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower than the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output. The output voltage is fed back through an internal resistor divider connected to V_{OUT1}/V_{OUT2} pins.

PG_LDO

PG_LDO is an open drain pulldown NMOS output that will sink 1mA at 0.4V max. It goes to the active low state if either LDO output is out of regulation by more than 15%. When the LDO is disabled, the output is active low.

Internal P-Channel Pass Transistors

Both ISL6413 LDO Regulators feature a typical 0.5Ω $r_{DS(ON)}$ P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6413 does not suffer from these problems.

Integrator Circuitry

Both ISL6413 LDO Regulators use external 33nF compensation capacitors for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown.

Current Limit

The ISL6413 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO1 is 330mA and LDO2 is 250mA. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Integrated RESET for MAC/Baseband Processors

The ISL6413 includes a microprocessor supervisory block. This block eliminates the extra RESET IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a RESET signal whenever the V_{IN} supply voltage decreases below a preset threshold, keeping it asserted for a programmable time (set by external capacitor CT) after the V_{IN} pin voltage has risen above the RESET threshold.

The push pull output stage of the reset circuit provides both an active-Low and an active-High output. The RESET threshold for ISL6413 is 2.630V typical.

UVLO Reset threshold is always lower than the RESET threshold. This insures that as V_{IN} falls, the reset goes low before the LDOs and PWM are shut off.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6413. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection protects the ISL6413 against fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Operating Region and Power Dissipation

The maximum power dissipation of ISL6413 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where

P1 = (I_{OUT} x V_{OUT}) x n, n is efficiency of the PWM

P2 = I_{OUT1} (V_{IN} - V_{OUT1})

P3 = I_{OUT2} (V_{IN} - V_{OUT2})

The maximum power dissipation is:

Pmax = (Tjmax – T_A)/θJA

Where Tjmax = 150°C, T_A = ambient temperature, and θJA is the thermal resistance from the junction to the surrounding environment.

The ISL6413 package features an exposed thermal pad on its underside. This pad lowers the thermal resistance of the package by providing a direct heat conduction path from the die to the PC board. Additionally, the ISL6413's ground (GND_LDO and PGND) performs the dual function of providing an electrical connection to system ground and channeling heat away. Connect the exposed backside pad direct to the GND_LDO ground plane.

Application Information

LDO Regulator Capacitor Selection and Regulator Stability

Capacitors are required at the ISL6413 LDO regulators' input and output for stable operation over the entire load range and the full temperature range. Use >1µF capacitor at the input of LDO regulators, V_{IN}_LDO pins. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provide better PSRR and line transient response. The input capacitor must be located at a distance of not more than 0.5 inches from the V_{IN} pins of the IC and returned to a clean analog ground. Any good quality ceramic capacitor can be used as an input capacitor.

The output capacitor must meet the requirements of minimum amount of capacitance and ESR for both LDO's. The ISL6413 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor, with a minimum value of 3.3µF, is recommended for V_{OUT1} for 300mA output current, and 3.3µF is recommended for V_{OUT2} at 200mA load current. There is no upper limit to the output capacitor value. A larger capacitor can reduce noise and improve load transient response, stability and PSRR. A higher value of output capacitor (10µF) is recommended for LDO2 when used to power VCO circuitry in wireless chipsets. The output capacitor should be located very close to V_{OUT} pins to minimize impact of PC board inductances and the other end of the capacitor should be returned to a clean analog ground.

PWM Regulator Component Selection

Inductor Selection

A 10µH typical output inductor is used with the ISL6413 PWM section. Values larger than 15µH or less than 8µH may cause stability problems because of the internal compensation of the regulator. The important parameters of the inductor that need to be considered are the current rating of the inductor and the DC resistance of the inductor. The DC resistance of the inductor will influence the efficiency of

the converter directly. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current.

TABLE 2. RECOMMENDED INDUCTORS

OUTPUT CURRENT	INDUCTOR VALUE	VENDOR PART #	COMMENTS
0mA to 600mA	10µH	Coilcraft DO3316P-103 Coilcraft DT3316P-103 Sumida CDR63B-100 Sumida CDRH5D28-100	High Efficiency
		Coilcraft DO1608C-100 Sumida CDRH4D28-100	Smallest Solution
0mA to 300mA	10µH	Coilcraft DS1608C-103	High Efficiency
		Murata LQH4C100K04	Smallest Solution

Output Capacitor Selection

For best performance, a low ESR output capacitor is needed. If an output capacitor is selected with an ESR value ≤120mΩ, its RMS ripple current rating will always meet the application requirements. The RMS ripple current is calculated as:

$$I_{RMS(C)_O} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \left(\frac{1 - \frac{V_O}{V_I}}{L \times f} \right) \times \left(\frac{1}{8 \times C_O \times f} + ESR \right)$$

Where the highest output voltage ripple occurs at the highest input voltage.

TABLE 3. RECOMMENDED CAPACITORS

CAPACITOR VALUE	ESR/mΩ	VENDOR PART #	COMMENTS
10µF	50	Taiyo Yuden JMK316BJ106KL	Ceramic
47µF	100	Sanyo 6TPA47M	POSCAP
68µF	100	Sprague 594D686X0010C2T	Tantalum

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes.

The input capacitor should have a minimum value of 10µF and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_{O(max)} \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)}$$

The worst case RMS ripple current occurs at 50% duty cycle.

Ceramic capacitors show good performance because of their low ESR value, and because they are less sensitive to voltage transients, compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the IC for best performance.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design of ISL6413 based power supply due to high switching frequency and low noise LDO implementations.

Allocate two board levels as ground planes, with many vias between them to create a low impedance, high-frequency plane. Tie all the device ground pins through multiple vias each to this ground plane, as close to the device as possible. Also tie the exposed pad on the bottom of the device to this ground plane.

Use wide and short traces for the high current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node to minimize the effects of ground noise.

Conclusion

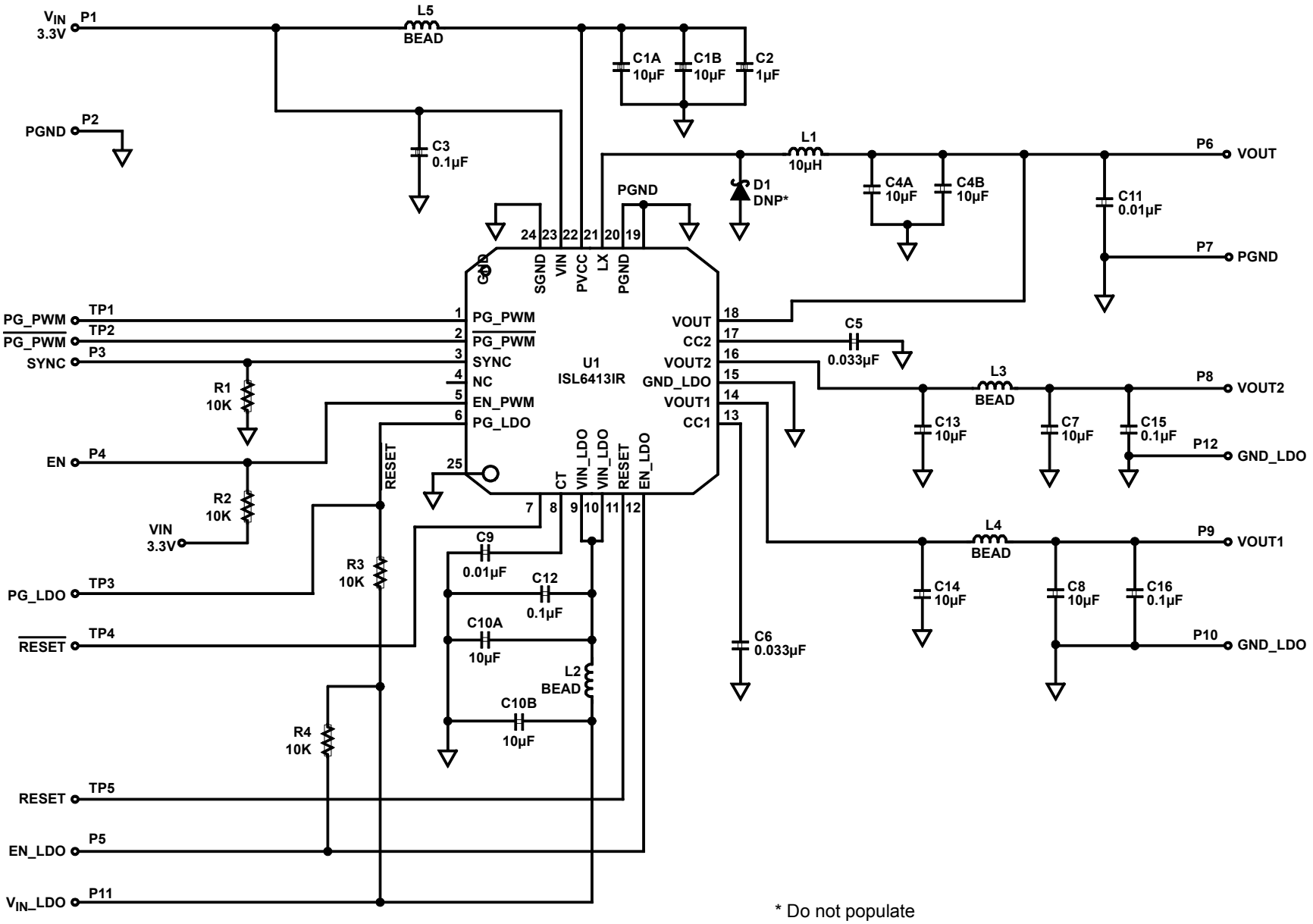
The ISL6413 is a system electronic regulator for 802.11 wireless chipset power management. The IC offers a significant power savings compared to LDO options and features small footprint and high integration, which make it an ideal single chip power solution for various 802.11 chipset power supplies.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6413 Data Sheet,* Intersil Corporation, File No. FN9129.

Evaluation Board Schematic ISL6413



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ISL6413 Evaluation Board Bill of Materials

ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL6413IR	IC, Linear, Multi-Output Regulator, Integrated Wireless Chipset		4x4 QFN	Intersil
2	L1	1	LQH32CN100K51L-T	Inductor	10µH, 10%	SM_1210	muRata
3	L2, L3, L4, L5	4	BLM21PG300SN1	Ferrite Bead	Chip EMI Filter	SM_0805	muRata
4	C1A, C1B, C4A, C7, C8, C10A, C10B, C13, C14	9	1210ZC106KAT2A	Capacitor, Ceramic, X7R	10µF, 10%, 10V	SM_1210	AVX
5	C2	1	0805ZC105KAT2A	Capacitor, Ceramic, X7R	1µF,10%,10V	SM_0805	AVX
6	C3, C12, C15, C16	4	0603ZC104KAT2A	Capacitor, Ceramic, X7R	0.1µF,10%,10V	SM_0603	AVX
7	C5, C6	2	0603ZC333JAT2A	Capacitor, Ceramic, X7R	0.033µF, 5%, 10V	SM_0603	AVX
8	C9, C11	2	0603ZC103KAT2A	Capacitor, Ceramic, X7R	0.01µF, 10%, 10V	SM_0603	AVX
9	C4B (DNP)		DNP			DO214	
10	R1 - R4	4		Resistor, Film	10kΩ, 5%, 0.1W	SM_0603	Digi-Key
11	D1 (DNP)	1	DNP	Diode Schottkey			
12	P1 - P12	12	1514-2	Turrett Post	Terminal post, through hole, 1/4 inch tall	PTH	Keystone
13	TP1 - TP5	5	5002	TEST POINT vertical, white	PC test jack	PTH	Keystone
14		4		Bumpers			

ISL6413 Evaluation Board Layout

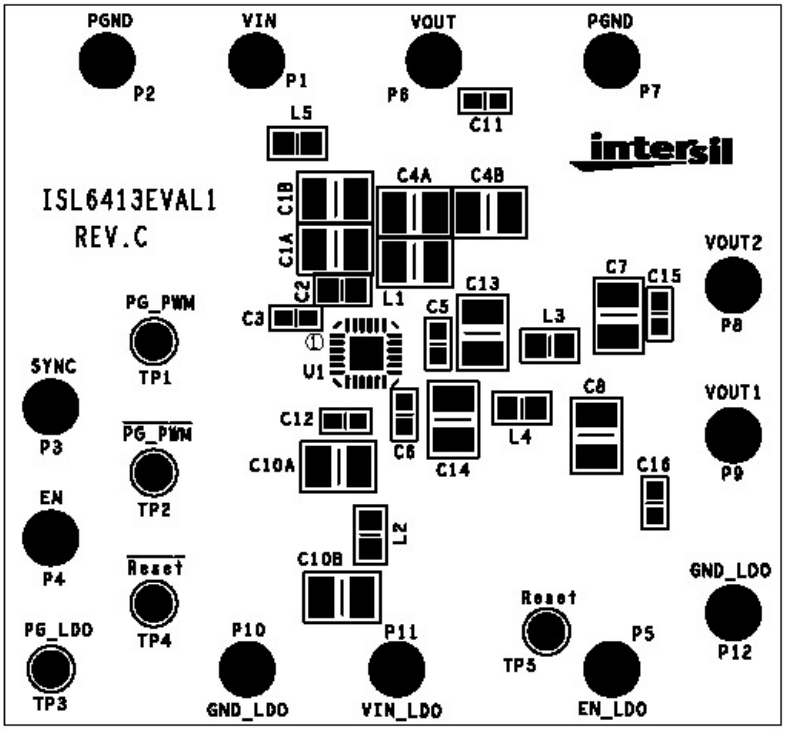

FIGURE 15. TOP SILK PRINT

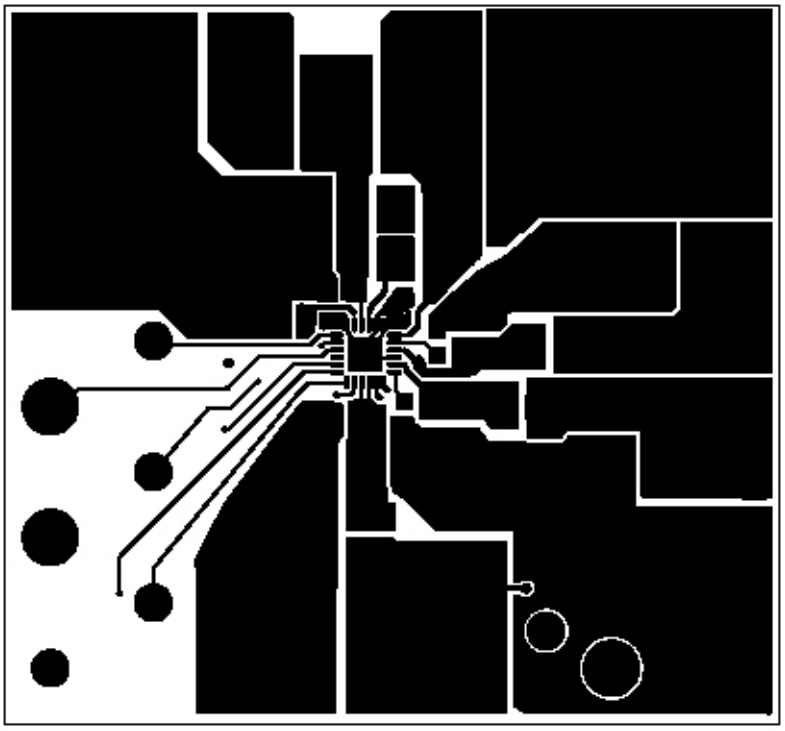

FIGURE 16. TOP LAYER

ISL6413 Evaluation Board Layout (Continued)

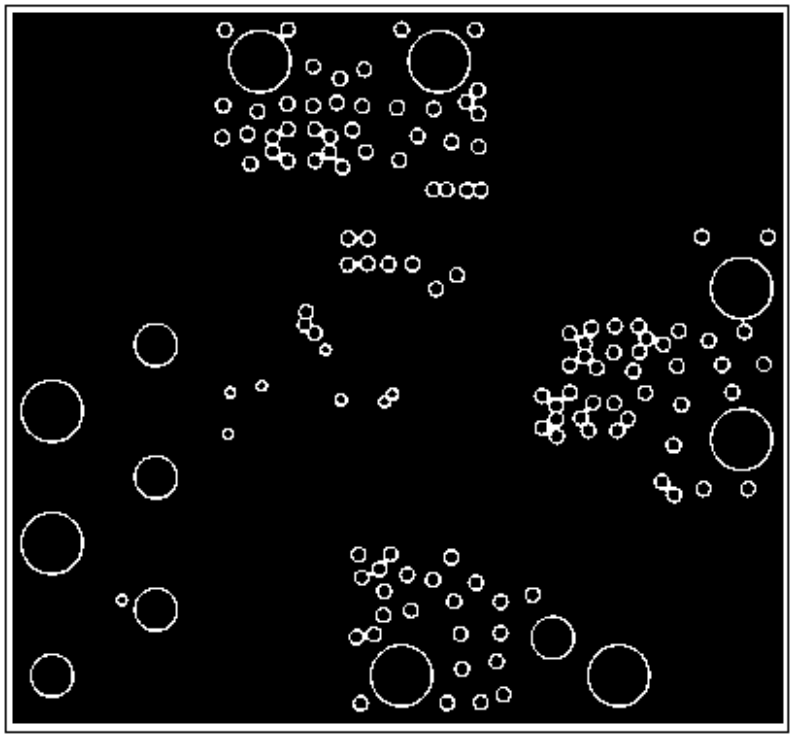

FIGURE 17. LAYER 2

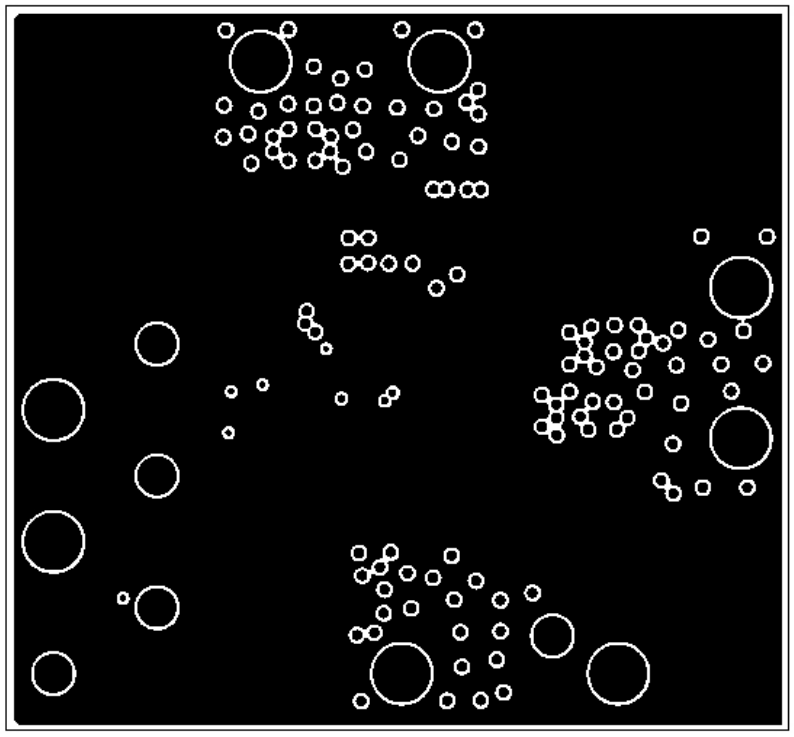

FIGURE 18. LAYER 3

ISL6413 Evaluation Board Layout (Continued)

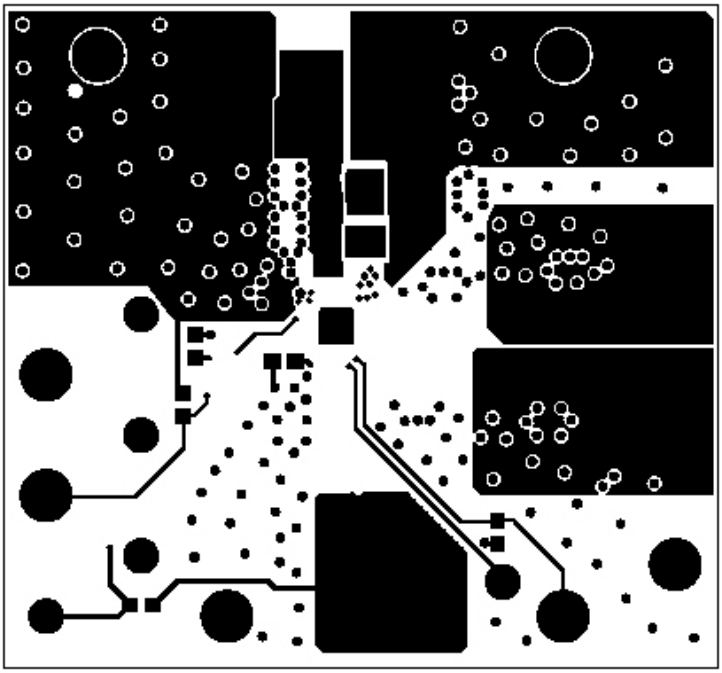

FIGURE 19. LAYER 4

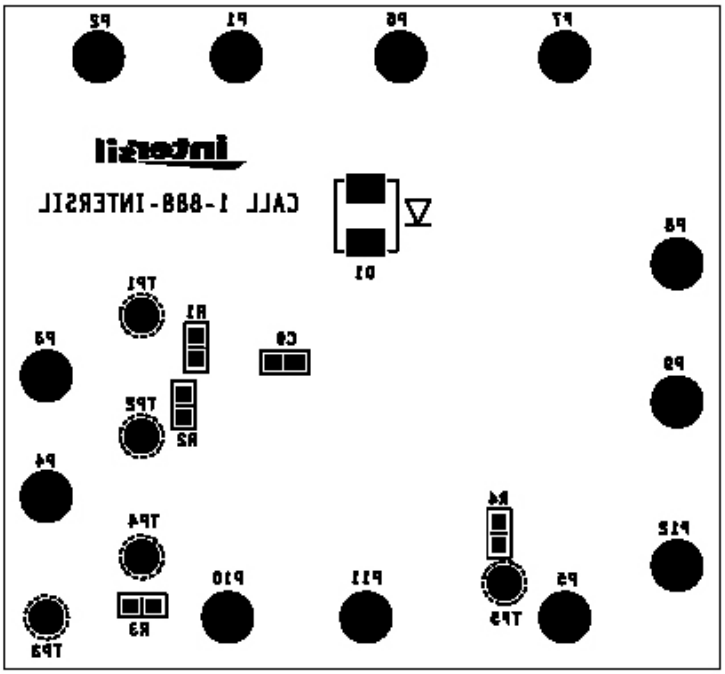

FIGURE 20. ISL6413 ENG1 - BOTTOM LAYER

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